In the Drawings:

Please amend Figures 6 and 6b as shown in the enclosures. Clean copies of amended Figures 6 and 6b (labeled as "Replacement Sheets") and marked-up copies of Figures 6 and 6b (labeled as "Annotated Sheets") showing the amendments in red are attached hereto.

REMARKS

The applicant has carefully considered the Office action dated November 23, 2005 and the references it cites. By way of this Response, claims 1, 4, 7, 9, 15, 17, 29, and 32 have been amended and claims 3, 6, 10, 20, and 30 have been cancelled without prejudice to their further prosecution. In view of the following, it is respectfully submitted that all pending claims are in condition for allowance and favorable reconsideration is respectfully requested.

As an initial matter, the applicant notes that claims 24-28 stand allowed and are not further discussed herein. Further, the Office action indicated that claims 30 and 32 would be allowed if rewritten in independent form. In accordance with this suggestion, claim 29 has been amended to incorporate the recitations of claim 30, and claim 32[1] has been rewritten in independent form. Accordingly, claims 29 and 32, as well as all claims depending therefrom, are in condition for allowance and will not be further discussed herein.

As a further initial matter, the applicant notes that, by way of this response, certain typographical errors have been corrected in the specification and drawings. No new matter has been entered.

Turning to the 35 U.S.C. § 101 rejections of claims 1 and 4, claim 1 has been amended to indicate that placing the cache line in the second cache in an enhanced exclusive state occurs *when* a copy of the cache line is in the first

[1] Claim 32 was rejected under 35 U.S.C. § 112. However, claim 32 was not indefinite as originally filed. However, to render this rejection moot, claim 32 has been broadened by removing the term "second" from the original phrase "a second snoop hit-modified signal." Accordingly, it is respectfully submitted that the objection to claim 32 should be withdrawn.

cache in a modified state and the cache line in the second cache is identical to a copy of the cache line in a main memory. Claim 4 has been amended to specify that the second cache memory places the cache line in an enhanced exclusive state *when* a copy of the cache line is in the first cache in a modified state and the cache line in the second cache is identical to a copy of the cache line in a main memory. In view of these amendments, it is respectfully submitted that the 35 U.S.C. § 101 rejections should be withdrawn.

Turning to the art rejections, the Office action rejected claims 1-23, 29 and 31 as being unpatentable over one or more of Albonesi et al., U.S. Patent 5,113,514, and Merrell et al., U.S. Patent 5,829,038. The applicant respectfully traverses these rejections.

Independent claim 1 recites a method comprising, among other things, placing a cache line in a second cache in an enhanced exclusive state when a copy of the cache line is in a first cache in a modified state and the cache line in the second cache is identical to a copy of the cache line in a main memory. Claim 1 also recited placing the cache line in the second cache in an enhanced modified state when a copy of the cache line may be in the first cache and the cache line in the second cache is different from the copy of the cache line in the main memory. None of the cited art teaches or suggests such a method.

Albonesi includes a modified state wherein a cache block in a secondary cache and/or a cache block in an operand cache associated with the secondary cache have been changed relative to the corresponding cache block in main memory. (Col. 9, lines 7-13). Thus, the Albonesi modified state is broadly defined to encompass the situation where either the cache block in the secondary cache or the cache block in the operand cache has been changed

relative to the cache block in the main memory. Further, Albonesi describes a private state wherein the secondary cache is the same as the corresponding cache block in main memory. (Col. 9, lines 4-7). However, Albonesi does not teach or suggest an enhanced exclusive state and an enhanced modified state as recited in claim 1.

As noted in applicant's specification (see, e.g., paragraph [0043]) and in the text of claim 1, the enhanced modified state is a state in which the cache line in a given cache (e.g., the second cache) is ***different*** from a copy of the cache line in main memory and a copy of the cache line may be in another cache (e.g., the first cache) in any state. In contrast, the private state described in Albonesi at Col. 9, lines 4-7 require the data in the cache block in the second cache to be the same as the cache block in the main memory. Since the second cache of claim 1 includes a cache line that is ***different from, not consistent with***, the cache line in main memory when in the enhanced modified state, it is clear that the private state of Albonesi is not an enhanced modified state as recited in claim 1. Therefore, Albonesi does not meet the recitations of claim 1.

Moreover, there is no teaching or suggestion for modifying Albonesi to incorporate an enhanced exclusive state and an enhanced modified state as recited in claim 1. Therefore claim 1 and all claims depending therefrom are in condition for allowance.

Independent claim 4 is also allowable. Claim 4 recites, among other things, a second cache memory that places a cache line in an enhanced exclusive state when a copy of the cache line is in the first cache memory in a modified state and the cache line in the second cache is identical to a copy of

the cache line in a main memory, and the second cache memory places the cache line in an enhanced modified state when a copy of the cache line may be in the first cache and the cache line in the second cache is different from the copy of the cache line in the main memory. As discussed in detail above, there is no teaching or suggestion for modifying Albonesi to include such cache memory. Therefore claim 4 and all claims depending therefrom are in condition for allowance.

Independent claim 7 is also allowable. Claim 7 recites, among other things, a method comprising (1) if a cache line is in an enhanced modified state, issuing an inquiry to a first cache; and victimizing the cache line in the second cache without a write-back of the cache line from the second cache if the response from the first cache is indicative of a cache hit; and (2) if the cache line is in a non-enhanced modified state, performing a write-back of the cache line from the second cache without issuing the inquiry to the first cache. In other words, there are two different modified states in claim 7. In one modified state (the enhanced modified state), an inquiry is issued to a first cache. In the second modified state (the non-enhanced modified state), no inquiry is issued to the first cache. No combination of the art of record teaches or suggests such a method.

For example, Merrell, assigned of record to the same assignee as the instant application, issues an inquiry whenever the cache line to be victimized is in a modified state (see blocks 202 and 203 of FIG. 2). There is no distinction made in Merrell between a modified state and an enhanced modified state. On the contrary, whenever the victimized line has been

modified (block 202), an inquiry is sent to the first cache. Accordingly, Merrell does not teach or suggest the method of claim 7.

There is no teaching or suggestion of modifying Merrell to meet the recitations of claim 7. Accordingly, claim 7 and all claims depending therefrom are in condition for allowance.

Independent claim 17 is also allowable. Claim 17 recites an apparatus comprising, among other things, a second cache memory structured to issue an inquiry to the first cache memory if a cache line to be victimized in the second cache memory is in an enhanced modified state, and to perform a write-back of the cache line from the second cache without issuing the inquiry to the first cache if the cache line is in a non-enhanced modified state. In other words, there are two different modified states in claim 17. In one modified state (the enhanced modified state), an inquiry is issued to a first cache. In the second modified state (the non-enhanced modified state), no inquiry is issued to the first cache. As explained above, no combination of the art of record teaches or suggests such an apparatus. Accordingly, claim 17 and all claims depending therefrom are in condition for allowance.

In view of the foregoing, it is respectfully submitted that all pending claims are in condition for allowance.

If the Examiner is of the opinion that a telephone conference would expedite the prosecution of this case, the Examiner is invited to contact the undersigned at the number identified below.

Respectfully submitted,

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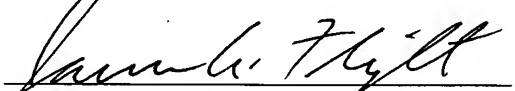
By: 
James A. Flight
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April 24, 2006

FIG. 6

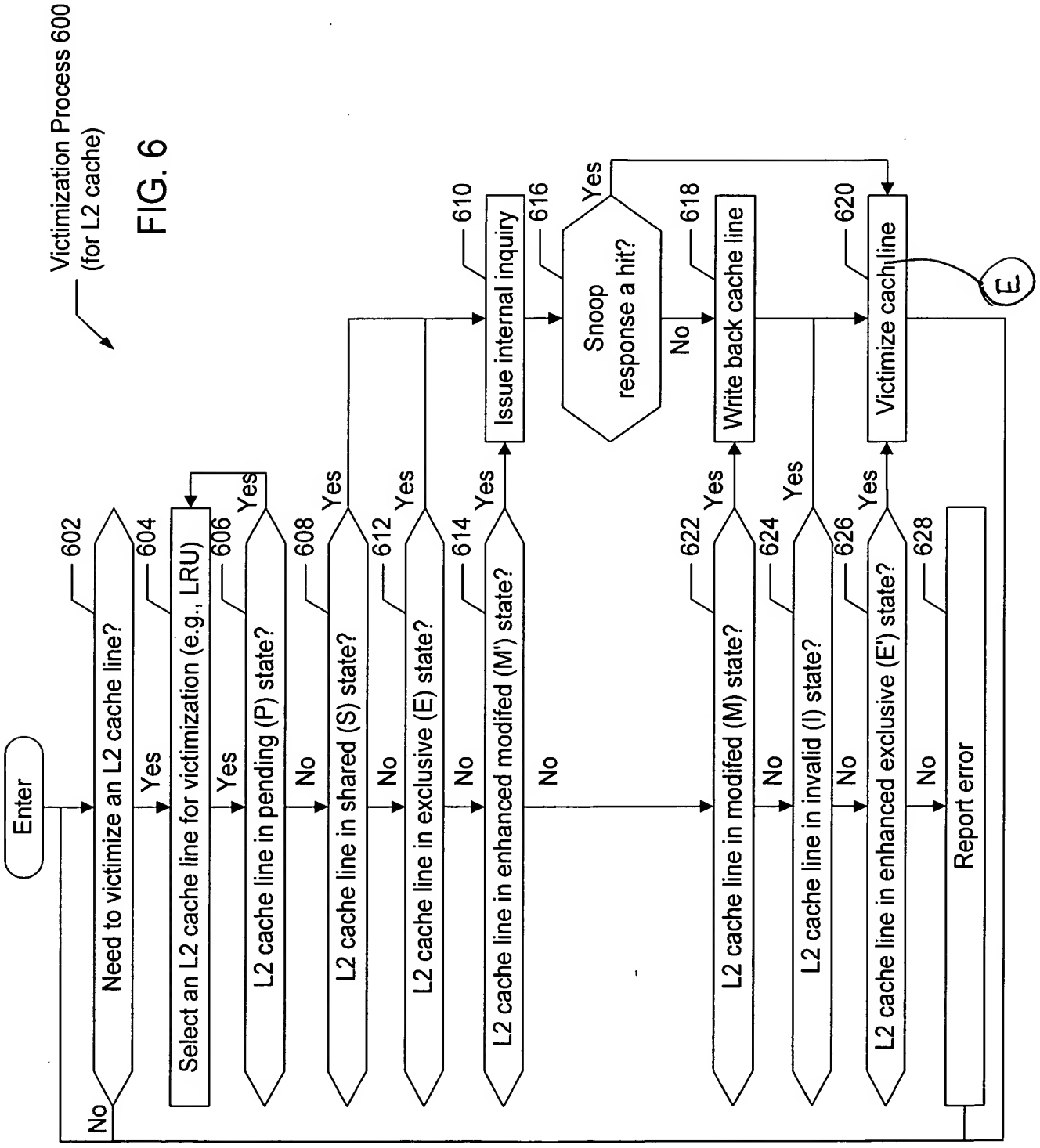

FIG. 6b